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February 25, 2002

GP/2812 #2
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J.W.B.
Zea

To: Commissioner of Patents and Trademarks
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Subject:

Serial No. 10/038,388 01/03/02

Hsiu-Mei Yu et al.

ELASTOMER PLATING MASK SEALED
WAFER LEVEL PACKAGE METHOD

Grp. Art Unit: 2812

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
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mail in an envelope addressed to: Commissioner of Patents and
Trademarks, Washington, D.C. 20231, on March 1, 2002.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Stephen B. Ackerman 3/1/02

U.S. Patent 5,994,152 to Khandros et al., "Fabricating Interconnects and Tips Using Sacrificial Substrates," discloses a mask for bump electroplating.

U.S. Patent 5,937,320 to Andricacos et al., "Barrier Layers for Electroplated SNPB Eutectic Solder Joints," discloses a bump process using a UMB and electroplating process.

U.S. Patent 5,767,010 to Mis et al., "Solder Bump Fabrication Methods and Structure including a Titanium Barrier Layer," discloses a method for fabricating solder bumps on a microelectronic device having contact pads.

Sincerely,

Stephen B. Ackerman
Stephen B. Ackerman,
Reg. No. 37761

Application Number

Group Art Unit

2812

[illegible][illegible][illegible]

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.